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Soft start-up strategy of pulse-density-modulated series-resonant converter for induction heating application

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ABSTRACT

This paper presents a soft start-up strategy of pulse-density-modulated series-resonant converter for induction heating application. The pulse-density modulation (PDM) technique is widely used in converters based on voltage-source series-resonant inverters (SRIs) to control the output current or power. However, during a start-up process, PDM has some disadvantages both in inrush current limiting and providing a zero-voltage switching operation of SRI transistors. In the paper, different PDM techniques are considered and basic moments of PDM using within the start-up process are analyzed. A new soft start-up strategy of PDM converter for induction heating application is proposed. The main features of the proposed strategy include an interleaved or a stepped PDM control, an initial combination of PDM at the beginning of the start-up process, and an operating algorithm during the start-up process. The proposed strategy was verified by a 2.5 kW experimental setup of the pulse-density-modulated interleaved converter with an operating frequency from 50 kHz up to 100 kHz. Experimental results confirm the effectiveness of the proposed start-up strategy and show that the maximum current amplitude within start-up processes exceeds the maximum steady-state current amplitude by no more than 30%.

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1. INTRODUCTION

Modern MOSFETs and IGBTs allow to create powerful high-frequency transistor converters. Such converters are increasingly used in various applications, in particular in induction heating systems. For these systems transistor converters based on the voltage-source or the current-source inverter are widely used. A start-up process is very important for transistor converters, especially to limit their inrush current. Furthermore, hard-switching operation modes of transistors under the start-up process may arise due to features of some control techniques. Therefore, the start-up process can be a difficult problem in power converters. Depending on which control technique is used to regulate the output current of the inverter, it is possible to obtain different switching modes of the inverter transistors both during the start-up process and in the steady-state mode. Many different control techniques have been proposed to regulate the output current or power of these converters, some of which make it possible to provide zero-voltage switching (ZVS) and/or zero-current switching (ZCS) operation modes. ZVS/ZCS makes it possible to substantially reduce power losses in the converters with high-frequency operation modes. The advantage of converters based on the voltage-source series-resonant inverter (SRI) is that they have a simple power circuit configuration and regulation of its output current or power can

be implemented in many ways: pulse-frequency modulation, pulse-width modulation, phase-shift control, pulse-density modulation (PDM), and combinations of the mentioned above methods or some of their variations [1]-[16].

In recent years, one of the most frequently used techniques for regulating output current in voltage-source SRIs is PDM [14]-[21]. The advantage of the PDM SRI is ZVS and quasi-ZCS [15], [22]. It should be noted that the SRI must operate with a lagging power factor so that the transistor commutation is completed before its current falls to zero [23]. Lossless snubbing circuits are often used to reduce electromagnetic interference in PDM SRIs [16], [22], [24]. The use of these circuits allows to reduce *dv*/*dt* and surge voltage across the transistor, as well as commutation losses of the SRI transistors. However, the use of the PDM technique has its disadvantages. The main one is the appearance of an SRI current amplitude fluctuation. This fluctuation affects the maximum voltage applied to the capacitor *C* of the series-resonant circuit, the switching modes of the SRI transistors, and the power loss in these transistors. Under low quality factor *Q* of the series-resonant circuit, it can be a significant problem. The authors of [16]-[18], [20], [25]-[27] deal with ways to reduce the current amplitude fluctuation by improving control methods on the basis of traditional PDM. Another disadvantage of PDM using is that at a frequency much higher than the resonant frequency of the series-resonant circuit it is possible to get NON-ZVS commutation modes, especially during the start-up process. A soft start-up process plays an important role in limiting the maximum value of the output current amplitude of the SRI, especially when the induction heating equipment works on a workpiece-free induction coil. In such a case, the amplitude of the inrush current may reach several times the steady-state current amplitude. The appearance of the excessive inrush current during start-up processes may cause the failure of the SRI transistors and/or overvoltage on the capacitor *C* before the control system is able to limit the current by one of the commonly used techniques.

An implementation option of the soft start-up process is the gradual voltage increase of the power source [28]. The main disadvantage of this approach is the need to have a regulated power source. Another option is the frequency-decreasing method [15], [29]. In this case, the initial frequency of the converter must be far from the resonant one. However, it is not always possible because the induction heating equipment is to operate over a wide frequency range. It is possible to use phase-shift control to provide soft start-up process, but in this case the initial frequency has also be higher than the resonant frequency to provide ZVS, and the lower the value of *Q* and higher the value of the inverter output current, the higher the initial frequency must be.

This article builds upon the ideas of our preliminary work presented in [30], that showed the key features of control to limit the inrush current of the PDM converter. This paper extends the analysis of PDM control techniques, in particular, comparing the interleaved PDM control with the stepped one for the modular converter, extends the discussion of the start-up process of the converter with PDM control technique for more in-depth investigation. The main contribution of this paper is a new soft start-up strategy of PDM converter for induction heating application. All steps of the proposed start-up strategy are presented through an algorithm. The main novelties of this strategy are as follows: 1) selecting the suitable PDM control technique and combinations of PDM parameters which provide fewer amplitude fluctuations and the free-wheeling interval duration of the converter output current; 2) using the modular converter based on the series connection of inverters, and using the interleaved or stepped PDM control for this converter; 3) the start-up process begins from the maximum frequency and with the selected initial combination of PDM parameters. Enhanced experimental validations are also provided to verify the performance of the proposed strategy.

2. SYSTEM DESCRIPTION AND OPERATION PRINCIPLE

2.1. System configuration

A load of induction heating equipment (an induction coil and a workpiece) is usually modelled as a series connection of the equivalent inductor *L* and equivalent resistor *R*, based on its analogy with respect to a transformer, and it is defined by values of the equivalent inductance *L* and equivalent resistance *R* as shown in Figure 1. The resistance *R* represents the resistance of an inserted workpiece into an induction coil and the resistance of the coil itself. The inductance *L* represents inductances of the workpiece, coil, and air gap between the workpiece and induction coil. Values of *R* and *L* depend on the coil and workpiece geometries and materials, operating frequency of the process and other parameters. In series-resonant circuits, the inductor *L* and the resistor *R* are connected in series with the capacitor *C*. Figure 1 shows the basic circuit configuration of the induction heating equipment based on the SRI. The configuration includes a diode bridge rectifier, a DC-filter, a full bridge series-resonant inverter (FB-SRI), a matching transformer, and a control system. The matching transformer is used for galvanic isolation and impedance matching. A blocking capacitor C_b is needed to avoid the appearance of the DC component on the primary winding of the matching transformer.

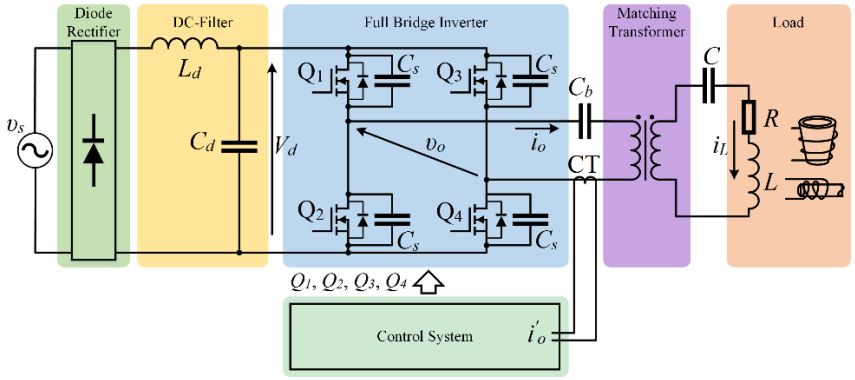


Figure 1. The basic circuit configuration of the induction heating equipment based on the SRI

2.2. Analysis of PDM techniques

Figure 2 depicts the PDM signal v_{PDM}, the gate control signals (Q_1, Q_2, Q_3, Q_4) of SRI transistors, and the voltage v_O and current i_O waveforms at the inverter output under PDM in the steady-state mode. The modulation period T_M of v_O contains two intervals: the ON-state time interval T_{ON} (PDM works by connecting the load to the source during m cycles of the period T_{sw} of v_O within T_{ON}) and the OFF-state interval T_{OFF} (PDM works on the short-circuited load during n cycles of T_{sw} within T_{OFF}). T_{ON} can also be named as an injection interval, because the energy on this interval is transmitted from the source into the series-resonant circuit; T_{OFF} can also be named as a free-wheeling interval, because at this interval the energy being stored in the capacitor C at the end of T_{ON} is dumped into the resistance R. The presence of these two intervals causes the amplitude fluctuation of i_O, and the lower the quality factor Q is, the greater is the fluctuation. The SRI output current or power regulation is carried out by changing the T_{ON} and T_{OFF} durations within T_M.

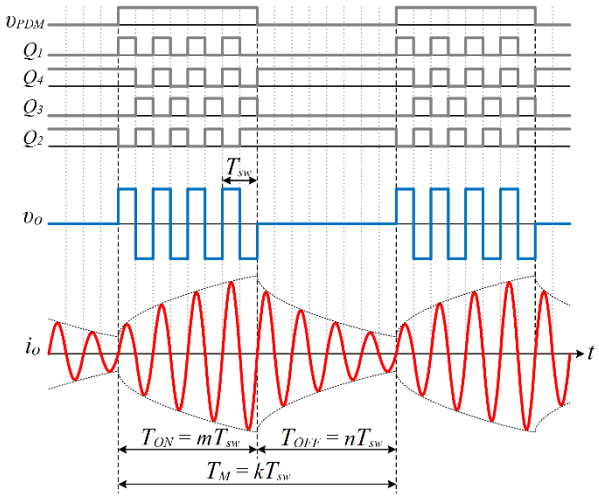


Figure 2. Pattern of drive sequences, voltage v_O and current i_O waveforms under the PDM operation

It is convenient to evaluate the modulation period T_M, interval T_{ON}, and interval T_{OFF} with the aid of numbers that are corresponded with the quantity of T_{sw} as shown in Figure 2:

$$m = T_{ON}/T_{sw},\ n = T_{OFF}/T_{sw},\ k = T_M/T \quad (1)$$

Where $k=m+n$ is a number of cycles having the period T_{sw} within T_M.

There are turn-off losses, no turn-on ones, and no reverse-recovery problem with antiparallel diodes in the case of operating with a lagging power factor [8], [23], [31]. This mode is preferred at high frequencies.

To make the switching process closer to optimum, it is advisable to change the dead-time T_{DT} between the SRI transistor control signals during the work process [6], [18]. In practice, under the steady-state mode the SRI operating frequency $\omega_{sw} = (2\pi)/T_{sw}$ is close to the resonance frequency $\omega_r = 1/\sqrt{LC}$ of the series-resonant circuit. The case of PDM technique in which m, n, and k are only integers, is often named in the literature as a "standard" or "traditional" PDM (Case I in Figure 3) [18], [20], [26]. The pulse density D of PDM can be expressed as (2)

$$D = T_{ON}/T_M = m/k \quad (2)$$

In [17], the PDM technique (where n are only integers, m and k are multiples of 0.5) for decreasing the amplitude fluctuation is analyzed in detail (Case II in Figure 3).

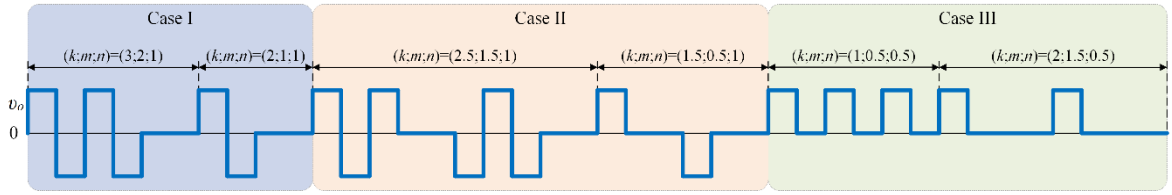


Figure 3. Waveforms of υ_O in case of different PDM techniques

The lowest amplitude fluctuation of i_O can be achieved when n and m are multiples of 0.5 and the value of k can be both an integer and a multiple of 0.5 as shown in Case III in Figure 3 [16], [18], [25]. In this case, most pattern variants of υ_O can be obtained, since such the case includes all the combinations (k; m; n) of the first two cases. Some authors name this PDM technique as "asymmetrical frequency modulation" (which is owing to the obtained pattern of υ_O) [16], other authors – as "enhanced pulse density modulation" (because smaller current amplitude fluctuations compared to the traditional PDM can be achieved) [18]. The authors of [20] this PDM case regard as one of three operation modes of their improved PDM and name this mode of operation as "semi mode". However, in this case, the voltage υ_O may contain a dc component. It should be paid a careful attention for choosing the capacitance of C_b. On the one hand, the larger value of C_b allows to reduce the maximum voltage on the primary winding of the matching transformer. On the other hand, this can lead to core saturation of the matching transformer under the change of (k; m; n) during operation and, especially, during the start-up process. This type of PDM is convenient when it is no need to use the matching transformer.

Both Cases II and III are advanced versions of the traditional PDM. The same density D can be achieved under different combinations of (k; m; n). Therefore, it is advisable to choose the combination of (k; m; n) providing the fewer free-wheeling interval and amplitude fluctuation of i_O [17], [25], [27]. In order to ensure a more uniform control characteristic, it is expedient to combine nearby combinations (k; m; n) to obtain additional characteristic points, and some of them can be excluded.

2.3. Drawback of PDM under Start-up Process

In order to provide ZVS operating during the start-up process, it is necessary to get a current lagging. For this purpose, it is advisable to set the initial frequency ω_{ini} of the SRI to the maximum, which has to be greater than ω_{sw}. Generally, a frequency tracking system for the SRI is based on a phase-locked-loop (PLL) technique that tracks the phase shift between υ_O and i_O. As a rule, this tracking system is realized by PLL-integrated circuits, digital controllers or field-programmable gate arrays [19], [32], [33]. It may be too high inrush current depending on: the value of ω_{ini} (how close it is to ω_{sw}), the quality factor Q, and the inertia of the control system for determining the error signal between the measured level of i_O and the task signal as shown in Figure 4(a). In this case, it is available to start work with the initial PDM combination to prevent an excessive high inrush current. The use of such a combination of PDM makes it possible to limit inrush current during start-up processes even if ω_{ini} is close to ω_{sw}.

However, if the frequency ω_{sw} during the steady-state mode is much lower than ω_{ini}, NON-ZVS commutation modes of inverter transistors during the start-up process may occur, in particular, reverse-recovery problems with antiparallel diodes as shown in Figure 4(b). This is because free damped current oscillations occur at the T_{OFF}, with frequency

$$\omega_d = \omega_r \sqrt{1-\xi^2} \quad (3)$$

Where $\xi = \frac{R}{2}\sqrt{\frac{C}{L}}$ is the damping factor.

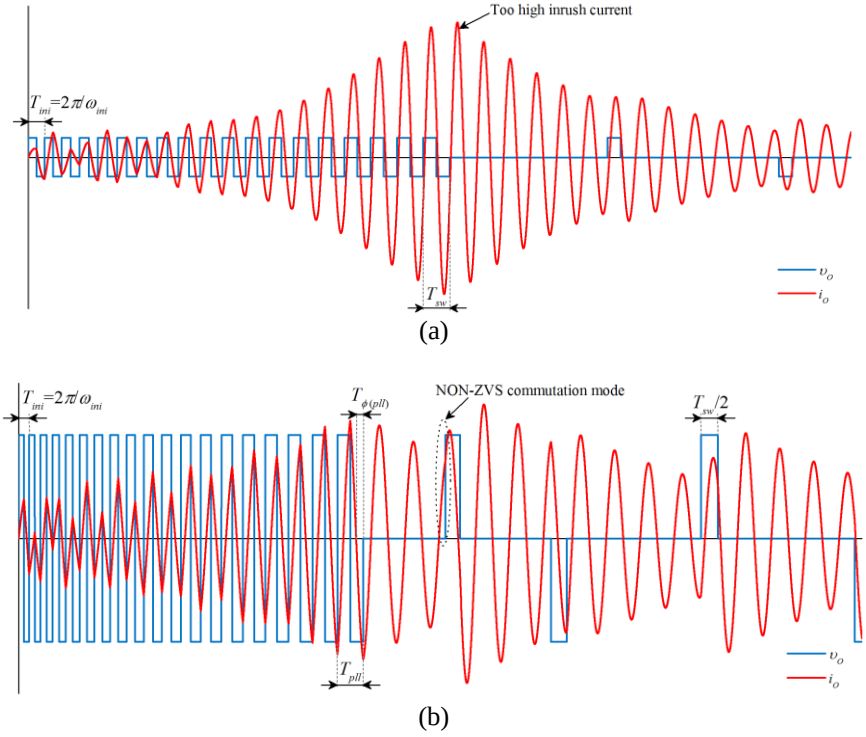


Figure 4. Waveforms of start-up processes under PDM, (a) ω_{ini} is close to ω_{sw}, (b) ω_{ini} is much higher than ω_{sw}

Within the start-up process, when the control system would start to use PDM, after T_{OFF} at the beginning of the next T_{ON} a time shift T_φ between υ_O and i_O will occur. The value of T_φ can be defined as

$$T_\varphi = 2\pi n\left(\frac{1}{\omega_d}-\frac{1}{\omega_{pll}}\right)+T_{\phi(pll)} \tag{4}$$

Where ω_{pll} is the fundamental frequency of υ_O at the beginning of T_{OFF}, $T_{\phi(pll)}$ is the time shift between the fundamental frequencies of υ_O and i_O at the beginning of T_{OFF}. NON-ZCS commutation modes of the transistors will occur provided that

$$T_\varphi \geq \frac{T_{pll}}{2} \rightarrow n \geq \frac{\frac{T_{pll}}{2}-T_{\phi(pll)}}{T_d - T_{pll}} \tag{5}$$

Where $T_d = 2\pi/\omega_d$ is the period of damped current oscillation, $T_{pll} = 2\pi/\omega_{pll}$ is the period of υ_O at the beginning of T_{OFF}. For providing ZVS operating it is necessary to compensate T_φ, for this the PLL tracking system during T_{OFF} has to make the frequency of its generator close to ω_d. In practice, under small values of n, this is a difficult task; in addition, the phase shift between υ_O and i_O is usually realized by the PLL system when changing of ω_{pll} is being fulfilled with the aid of the proportional-integral (PI) control.

2.4. Interleaved and stepped PDM controls

To reduce the current amplitude fluctuation and the duration of the free-wheeling interval, it is advisable to use an interleaved PDM control [20], [34], [35]. This kind of PDM control is suitable for converters

which are based on series or parallel connection of inverters. The use of interleaving between the PDM control of each channel of a modular converter to reduce the voltage ripple is considered in [20] and to increase the frequency of the converter – in [34]. The basic idea of the interleaved PDM control is that each channel of N inverters has the same pattern of the PDM signals and there is the time shift S between them; besides, the latter is the multiple of T_{sw}. Figure 5 shows a modular converter based on the series connection of two SRIs (N=2) and Figure 6 depicts the output voltages of each channel (v_{O1}, v_{O2}), load current (i_L), and total output voltage of the modular converter v_{total} under interleaved PDM. The pattern of v_{total} depends on the number N of series-connected inverters and the shift S between their PDM signals.

In Figure 6 it is shown the dependence of the v_{total} pattern on several combinations of (k; m; n) and different values of S. Providing of S allows to decrease the durations of the free-wheeling interval of i_L and output currents of inverters (i_{O1}, i_{O2}), respectively, as well as to decrease their amplitudes fluctuations. Under different values of S and the same combination of (k; m; n) the results may be the same or different. It is advisable to choose S in such a way to provide the least free-wheeling interval and amplitude fluctuation.

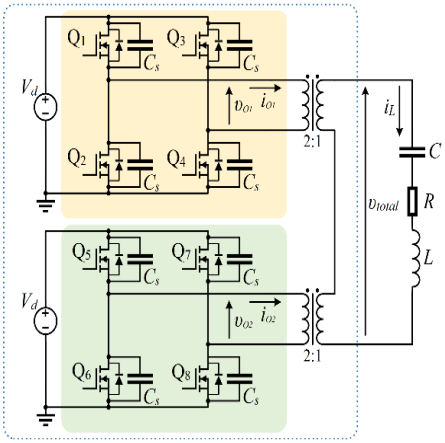


Figure 5. Modular converter based on the series connection of two SRIs

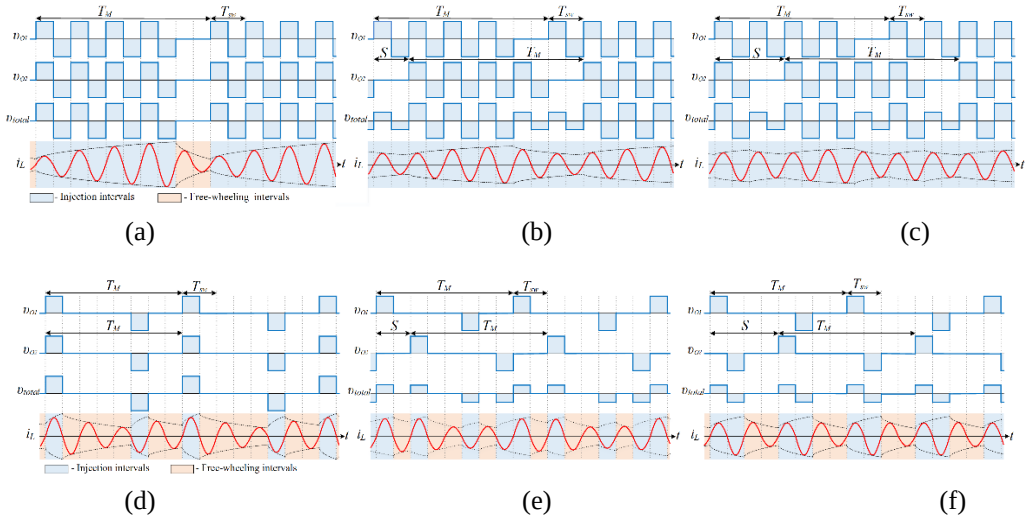


Figure 6. Voltage waveforms of v_{O1}, v_{O2}, and v_{total}, and current waveforms of i_L in case of: (a) (k;m;n)=(5;4;1) and S=0; (b) (k;m;n)=(5,4,1) and S=1; (c) (k;m;n)=(5;4;1) and S=2; (d) combained (k;m;n)=(2.5;0.5;2) with (k;m;n)=(1.5;0.5;1) and S=0; (e) combained (k;m;n)=(2.5;0.5;2) with (k;m;n)=(1.5;0.5;1) and S=1; (f) combained (k;m;n)=(2.5;0.5;2) with (k;m;n)=(1.5;0.5;1) and S=2.

The similar pattern of v_{total} can be obtained without interleaving of patterns of the PDM signals, but with the different patterns of PDM signals of each channel. In this case, to reduce the current amplitude fluctuation, it is advisable that the modulation is only in one of the N channels and the modulation signals in

the other ones are 0 and/or 1. This kind of modulation can be named as "stepped PDM" since modulation begins to act only in one channel, and when the modulation signal in this channel becomes steady-state 0, the modulation starts to act in other channel, and so on to the last of the *N* channels. In Figure 7 it is shown how to obtain the same pattern of υtotal when the interleaved or stepped PDM controls is being used. Anyway, using these kinds PDM allows to reduce the free-wheeling interval of i_L or avoid it at all.

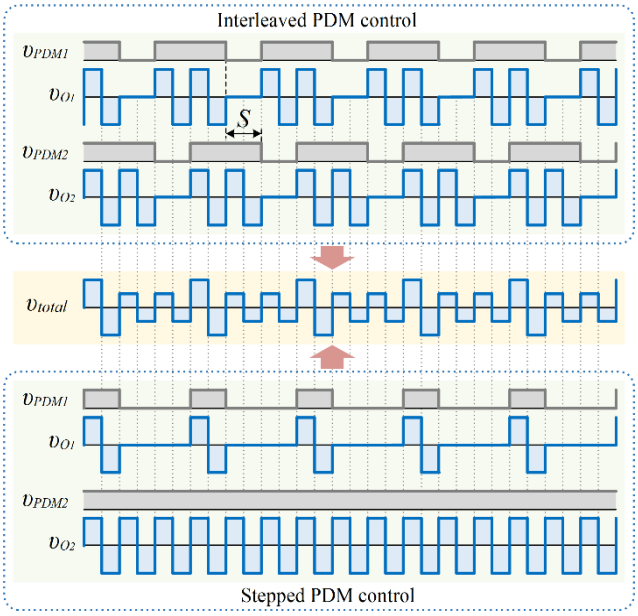


Figure 7. Interleaved PDM control vs. stepped PDM control

3. THE PROPOSED START-UP STRATEGY OF PDM CONVERTER

As stated in Section 2.2, the inverter output current can be controlled by different PDM techniques. For these techniques there can be selected combinations of (*k*; *m*; *n*) which provide a fewer free-wheeling interval. The analysis conducted in Section 2.3 revealed that the use of PDM in the start-up process can lead to NON-ZVS commutation modes of the transistors, in particular – switching of the SRI transistors onto open anti-parallel diodes, due to the difference between the frequencies ω_{pll} and ω_{sw}, and also the duration of the free-wheeling interval. In addition, it was shown that the use of the interleaved or stepped PDM control reduces the duration of the free-wheeling interval. In this section, on the basis of the analysis conducted above, the algorithm of the soft start-up strategy for PDM converter to provide ZVS of transistors and limiting the inrush current of the converter is proposed as shown in Figure 8. The strategy consists of the following steps:

1) Selecting the PDM technique to control i_L:
   - traditional PDM (Case I) – has high amplitude fluctuation of i_L, long duration of the free-wheeling interval, and is simple to implement;
   - enhanced PDM (Case II) – has fewer amplitude fluctuation of i_L, and less duration of the free-wheeling interval comparting with traditional PDM, but is more complex to implement;
   - enhanced PDM (Case III) – has the fewest amplitude fluctuation of i_L, and less duration of the free-wheeling interval, but there is a DC component of v_O.
2) Selecting combinations (*k*; *m*; *n*) (for the combinations with the same *D* preference has to be given to the combination with the smaller value of *n*; some of the combinations (*k*; *m*; *n*) can be combined to get additional points and some can be excluded).
3) Using an *N*-channel modular converter (based on the series connection of *N* inverters) and using the interleaved or stepped PDM control for this converter. The more channels modular converter contains, the fewer are the fluctuation level of i_O and the duration of the free-wheeling interval and the higher is the cost of the converter.
4) In the case of using the interleaved PDM control–for the selected combinations (*k*; *m*; *n*) determining the shift *S* which provides a fewer duration of the free-wheeling interval of i_L.

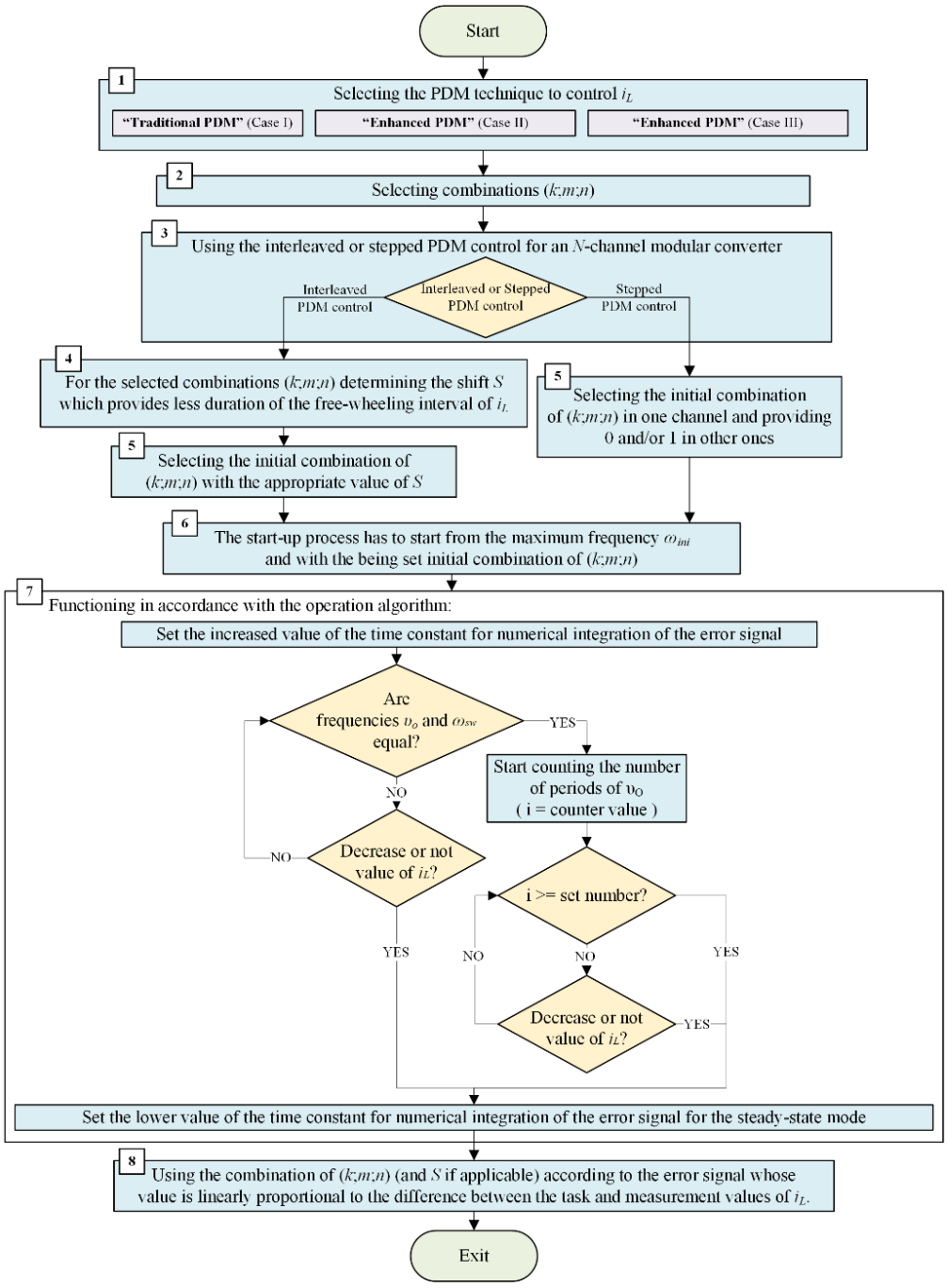


Figure 8. Algorithm of the proposed start-up strategy of PDM converter

5) In the case of using the interleaved PDM control – selecting the initial combination of (*k*; *m*; *n*) with the appropriate value of *S*. In the case of using the stepped PDM control – selecting the initial combination of (*k*; *m*; *n*) in one channel and providing 0 and/or 1 in other ones.
   Initial combination of (*k*; *m*; *n*) with the shift *S*, in the case of the interleaved PDM control, or initial combination of (*k*; *m*; *n*) in one channel with 0 and/or 1 in other ones, in the case of using the stepped PDM control, must be selected so that in the case of starting on the workpiece-free induction coil, the inrush current would be limited at an acceptable level.
6) The start-up process has to start from the maximum frequency ω_{ini} and with the being set initial combination of (*k*; *m*; *n*).
7) Functioning in accordance with the operation algorithm which is depicted in Figure 7.

Step 7 of the proposed strategy is executed during the interval when the PLL system changes the frequency of its generator from ω_{ini} to ω_{sw}. In this step, the error signal value must be considered only if it matches the combination (k; m; n) with the pulse density D less than that of the initial combination. Also, during this step within a set number of periods of v_O (when the frequency of v_O reaches ω_{sw}), the value of the time constant for numerical integration of the error signal has to be larger than its value during the steady-state mode. These two points are due to the fact that the initial combination can be replaced by a combination that will not be able to limit the inrush current to the desired level due to the inertia of measuring the value of i_L by the control system.

8) Using the combination of (k; m; n) and S according to an error signal whose value is linearly proportional to the difference between the task and measurement values of i_L.
Step 8 is the last step of the proposed strategy; it corresponds to the beginning of the steady-state mode. In the steady-state mode the control system continues to operate in accordance with this step and the selected PDM technique, PDM parameters, and interleaved/stepped PDM control.

As the inverters are connected in series with matching transformers, the output currents of the inverters are equal (i_{O1}=i_{O2}=i_O) and i_O is connected with i_L trough the transformer turns ratio. To provide ZVS operating modes, it is important to control phase-shift between v_O and i_O. Therefore, it is expedient to measure and regulate the value of i_O.

4. IMPLEMENTATION AND EXPERIMENTAL RESULTS

4.1. Experimental Setup and its Specifications

The experimental setup of the interleaved PDM converter was used to experimentally verify the effectiveness of the proposed start-up strategy [30]. The schematic depiction of the setup is illustrated in Figure 9. The setup works with an operating frequency from 50 kHz up to 100 kHz, contains two channels of FB-SRIs (N=2) and has total output power up to 2.5 kW. The setup is powered by the 220 VAC 50 Hz main. Each of the FB-SRIs uses four SiC MOSFETs (SCT3120ALGC11). The control system is based on the STM32H743ZIT6 microcontroller (MC). The transformation ratio of each matching transformer is 64:1. Main specifications of the experimental setup are summarized in Table 1.

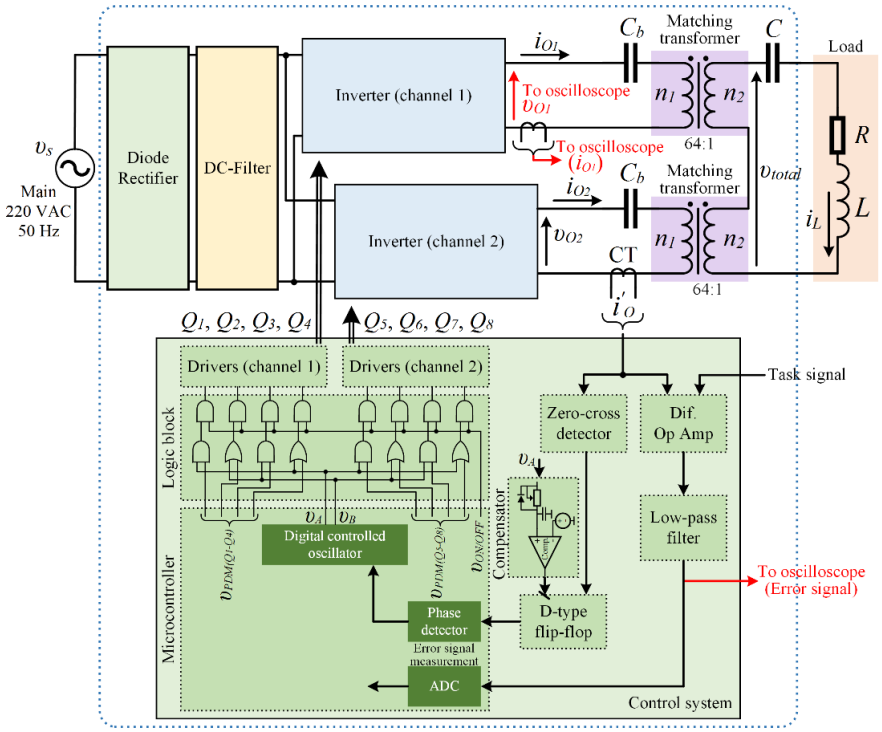


Figure 9. Schematic depiction of the experimental setup

Digital controlled oscillator (DCO) of MC forms two complimentary signals υ_A and υ_B with the constant value of the dead-time T_{DT} = 500ns. MC forms four PDM signals $\upsilon_{PDM(Q1\text{-}Q4)}$ for the first channel and four PDM signals $\upsilon_{PDM(Q5\text{-}Q8)}$ for the second channel of the converter. The PDM signals $\upsilon_{PDM(Q5\text{-}Q8)}$ repeat $\upsilon_{PDM(Q1\text{-}Q4)}$ with the shift S in accordance with PDM combination given in Table 2. Signals υ_A, υ_B, $\upsilon_{PDM(Q1\text{-}Q4)}$, and $\upsilon_{PDM(Q5\text{-}Q8)}$ are coming to the logic block where transistor signals are formed. The drivers are used for current amplifying of output signal of the logic block as well as for its galvanically isolation. The signal $\upsilon_{ON/OFF}$ is used to completely turn off, if necessary, all transistors of the converter (for inactive or emergency state). The load current i_L is connected with the output currents (i_{O1}, i_{O2}) of the converter's channels by the matching transformers. These currents are monitored by measuring the current of one channel (i'_O) with the current transformer. Load current regulation is carried out in accordance with the error signal value by PI control. The average value of the error signal is linearly proportional to the difference between the set value of the task signal and measured value of the output current. The error signal is then being passed through a low-pass filter as shown in Figure 8. A phase-locked loop (PLL) system is implemented with the aid of the MC as shown in Figure 10. This system uses a D-type flip-flop and a compensator, the latter is used to compensate the propagation delay between υ_A and υ_{O1} signals, as well as to provide the desired time shift between i_{O1} and υ_{O1}. The D-type flip-flop clamps the logic signal of the zero-current detector by the rise edge of the output signal of the compensator. Based on the signal from the D-type flip-flop, the MC changes the operating frequency by increasing/decreasing the counter value of DCO [19].

Table 1. Parameters of the Experimental Setup

Item	Symbol	Value
AC main	υ_s	220 VAC 50 Hz
Number of inverter channels	N	2
Rated output power (each channel)	P	2.5 kW (1.25 kW)
Operating frequency	f_{sw}	50-100 kHz
Transformer turns ratio of each channel	n_1:n_2	64:1
Capacitor	C	0.033 µF × 370 = 12.21 µF

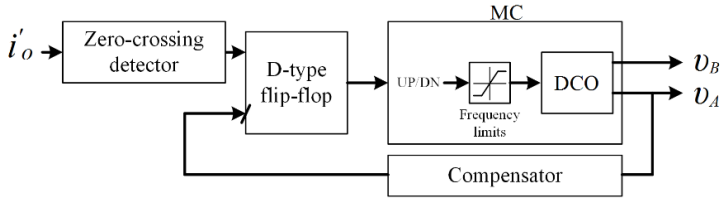


Figure 10. Block diagram of the PLL system.

Figure 11 presents two photographs of the experimental setup used in the described below experiments.

Figure 11. The experimental setup of the interleaved PDM series-resonant converter

The selected and stored in MC memory combinations of (k; m; n) and their shifts S are shown in Table 2. Some of the combinations have been obtained by combining two nearby combinations. The combination of (k; m; n) = (1.5;0.5;1) has been used by the control system as the initial one.

Table 2. PDM combinations (k; m; n) and shifts S stored in the MC

D	(k; m; n)	S
1	(10;10;0)	0
0.94	(16;15;1)	8
0.9	(10;9;1)	5
0.86	(7;6;1)	4
0.83	(6;5;1)	3
0.8	(5;4;1)	2
0.75	(4;3;1)	2
0.67	(3;2;1)	1
0.6	combining (3;2;1) and (2;1;1)	1
0.5	(2;1;1)	1
0.4	combining (1.5;0.5;1) and (2;1;1)	1
0.33	(1.5;0.5;1)	1
0.25	combining (2.5;0.5;2) and (1.5;0.5;1)	1
0.2	(2.5;0.5;2)	1
0.17	combining (3.5;0.5;3) and (2.5;0.5;2)	1
0.14	(3.5;0.5;3)	1
0.13	combining (4.5;0.5;4) and (3.5;0.5;3)	2
0.11	(4.5;0.5;4)	2
0.09	(5.5;0.5;5)	3
0	(10;0;10)	0

4.2. Experimental Waveforms and Results

Figure 12 shows the experimental waveforms of the error signal and output current in one of two setup's channels. The waveforms have been obtained under three different load conditions: Condition I – a workpiece is placed in an induction coil and the setup works almost with the full rated output power, $Q \approx 6.5$ as shown in Figure 12(a); Condition II – the workpiece is placed in the induction coil, but its equivalent resistance is less than that in the first case, $Q \approx 8$ as shown in Figure 12(b); Condition III – the setup works on the workpiece-free induction coil, $Q \approx 19.5$ as shown in Figure 12(c).

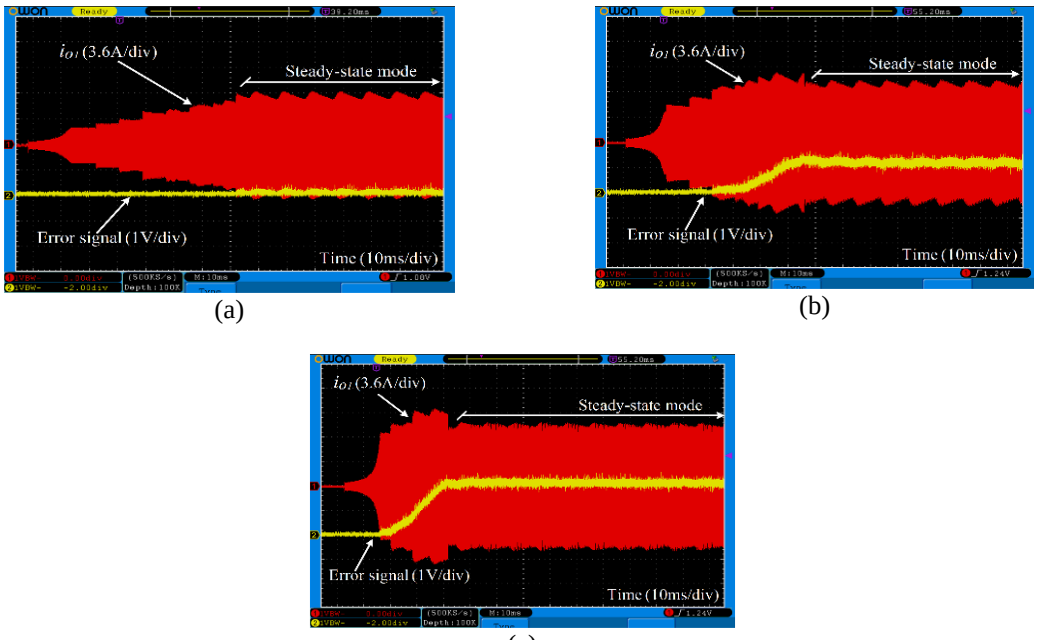


Figure 12. Experimental waveforms of i_{O1} and error signal in case of different load conditions, (a) Condition I, (b) Condition II, (c) Condition III

As it can be seen from these waveforms, the current amplitudes within the start processes are not much higher than they are within the steady-state mode. There is no an excessive inrush current in the case of Condition I, as shown in Figure 12(a) and the current rise is gradual. In the case of Condition II as shown in Figure 12(b) the maximal value of the inrush current does not greatly exceed the maximal amplitude of the current under the steady-state mode. The case of Condition III as shown in Figure 12(c) is the worst because the value of the inrush current is the maximal. But even in this case its value is not much higher than the maximal steady-state current amplitude, and the maximum current amplitude within start-up processes exceeds the maximum steady-state current amplitude by no more than 30%. It can be asserted that such limitation of the inrush current is enough to limit the maximum amplitude of the current through the converter transistors and the maximum voltage across the capacitor *C*. It is possible to add more channels to the converter to further reduce the inrush current. So, it can be argued that the proposed start-up strategy of the PDM converter is very useful, as it is evidenced by the obtained experimental waveforms of the inverter output current.

Figure 13 shows the waveforms of switch i_{O1} and v_{O1} under the steady-state mode for the mentioned above load conditions. There are no problems with commutation of SRI transistors, because it occurs in ZVS and quasi-ZCS commutation modes. The set value of T_{DT} is enough to ensure that there are ZVS/quasi-ZCS commutation modes under deep current regulation within the operating frequency range as shown in Figure 14.

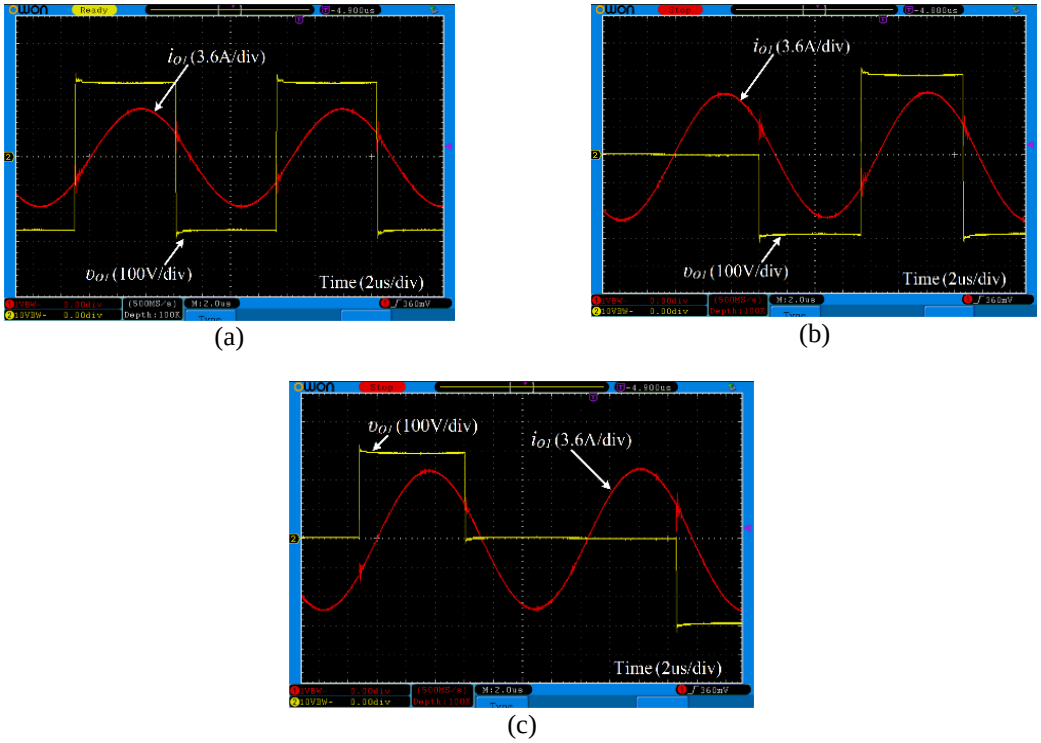
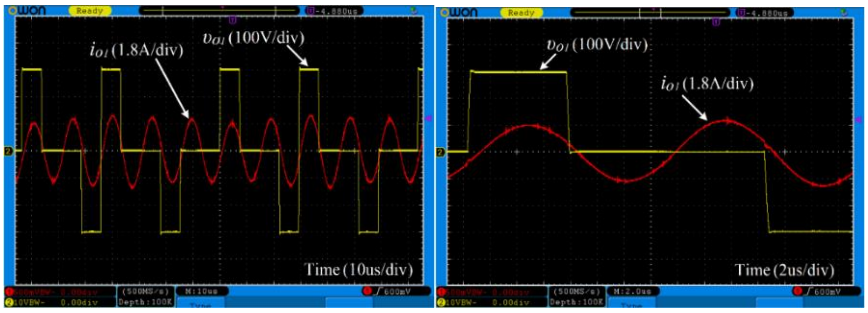


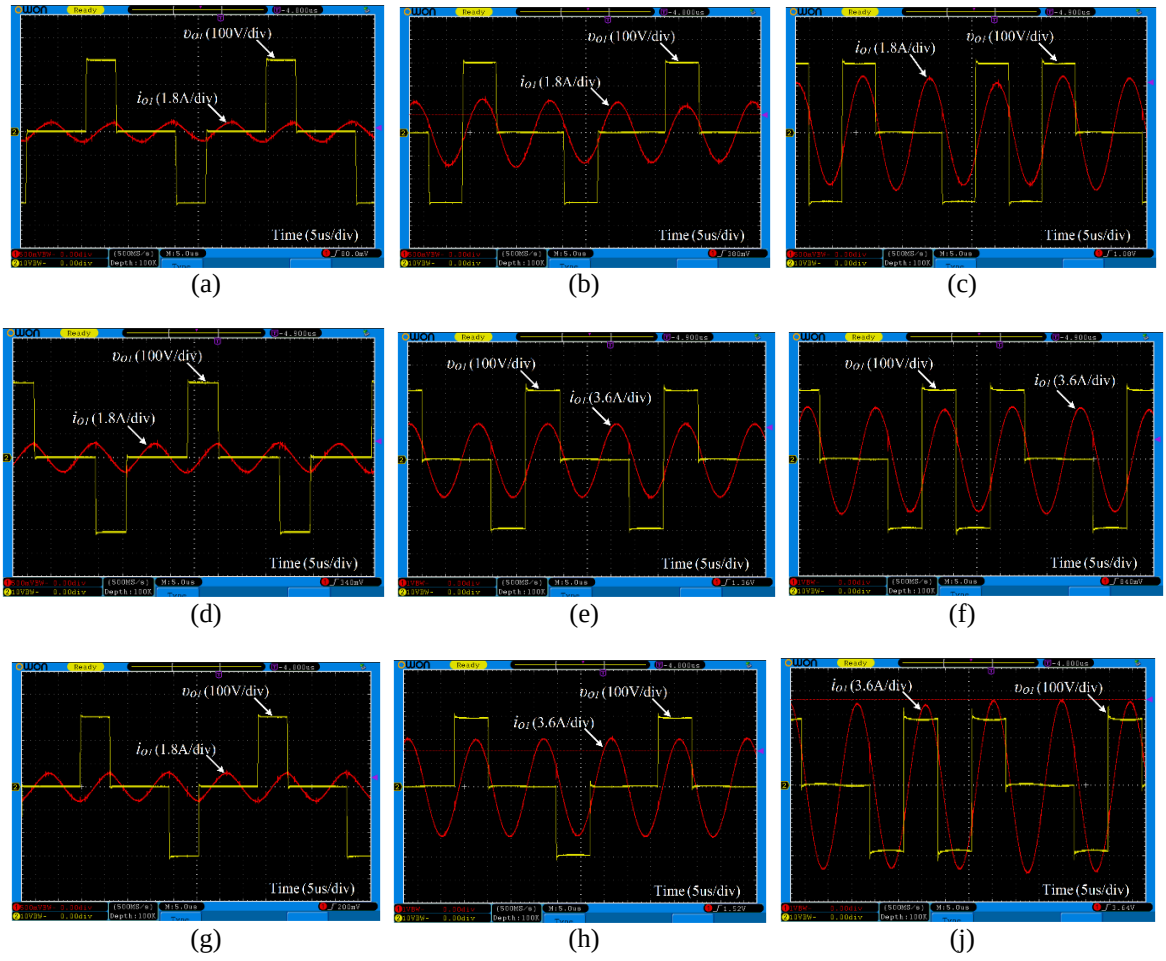
Figure 13. Experimental waveforms of i_{O1} and v_{O1} in steady-state mode,
(a) Condition I (D=1). (b) Condition II (D=0.8). (c) Condition III (D=0.33)

Figure 15 shows experimental waveforms of switch i_{O1} and v_{O1} within start-up processes for the mentioned above load conditions. There are also no problems with commutation modes of the transistors. Therefore, the start-up process may be considered as "soft". In the experiments described above the operation frequency under the steady-state mode was in the frequency range of 68 kHz to 71 kHz, depending on the workpiece of the induction coil. The initial frequency of the control system was equal to the maximum frequency of the operating range.



(a) (b)

Figure 14. Experimental waveforms of i_{O1} and v_{O1} in steady-state mode for Condition I under deep current regulation, (a) time 10us/div, (b) time 2us/div



(a) (b) (c)

(d) (e) (f)

(g) (h) (j)

Figure 15. Experimental waveforms of i_{O1} and v_{O1} within start-up process, (a)-(c) Condition I, (d)-(f) Condition II, (g)-(h) Condition III

5. CONCLUSION

This paper has proposed the soft start-up strategy of the PDM series-resonant converter for induction heating application. The main features of the proposed strategy include using the interleaved or stepped PDM control, the initial combination of PDM at the beginning of the start-up process, and the described above operating algorithm during the start-up process. The proposed algorithm of the start-up strategy allows to obtain limiting of the inrush current during the start-up process with zero-voltage switching commutation modes of the converter transistors. As a result, the output current of series-resonant converter and voltage across the

capacitor of the resonant circuit during the start-up process are limited, and the maximum current amplitude within start-up processes exceeds the maximum steady-state current amplitude by no more than 30%. It is possible to add more channels to the converter to further reduce the inrush current. It has been verified with the aid of the 2.5 kW experimental setup of the interleaved PDM converter that the proposed soft start-up strategy makes it possible to limit the maximal value of the inrush current and ensure zero-voltage switching operating under the start-up process.

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